

# IR 3/16 Encode/Decode IC

## Technical Data

### Features

- **Compliant with IrDA Physical Layer Specs**
- **Interfaces with IrDA Compliant HSDL-1000 IR Transceiver**
- **1 Micron CMOS Gate Array**
- **Used in Conjunction with Standard 16550 UART**
- **Pin Compatible with PLX-1000**

### Applications

#### Interfaces with HSDL-1000 to perform:

- **Serial Half-Duplex Data Transfer Between:**
  - Notebook Computers
  - Subnotebooks
  - Desktops PCs
  - PDAs
  - Printers
  - Other Peripheral Devices
- **Telecom Applications in:**
  - Modems
  - Fax Machines
  - Pagers
  - Phones
- **Industrial Applications in:**
  - Data Collection Devices
- **Medical Applications in:**
  - Patient and Pharmaceutical Data Collection

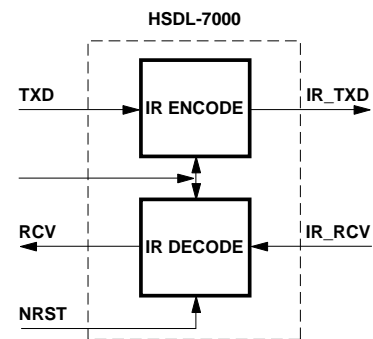
### Description

The HSDL-7000 performs the modulation/demodulation function used to both encode and decode the electrical pulses from the IR transceiver. These pulses are then sent to a standard UART which has a BAUDOUT signal available externally. This signal is 16 times the selected baud rate. In applications where the 16XCLK is not available, an external means of generating the 16XCLK must be designed.

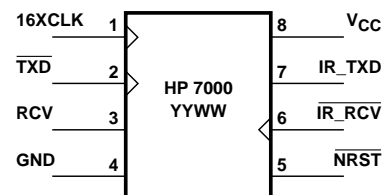
The HSDL-7000 is comprised of two state machines – the serial IR encode and the serial IR decode blocks. Each of these blocks derives their timing from the 16XCLK input signal from the UART. The Encode block is driven by the negative edge triggered TXD signal from the UART. This initiates the modulation state machine resulting in the 3/16 modulated IR\_TXD signal which drives the IR transceiver module, HSDL-1000. The IR Decode block is driven by the negative edge triggered IR\_RCV signal from the HSDL-1000. After this signal is demodulated and stretched, it drives the RCV signal to the UART.

## HSDL-7000

### Schematic



### Pin Out



## Pin Description

**16XCLK** - Positive edge triggered input clock that is set to 16 times the data transmission baud rate. The encode and decode schemes require this signal. The signal is usually tied to a UART's BAUDOUT signal.

**TXD** - Negative edge triggered input signal; usually tied to a UART's SOUT signal (serial data to be transmitted).

**RCV** - Output signal which is usually tied to a UART's SIN signal (received serial data).

**GND** - Chip ground.

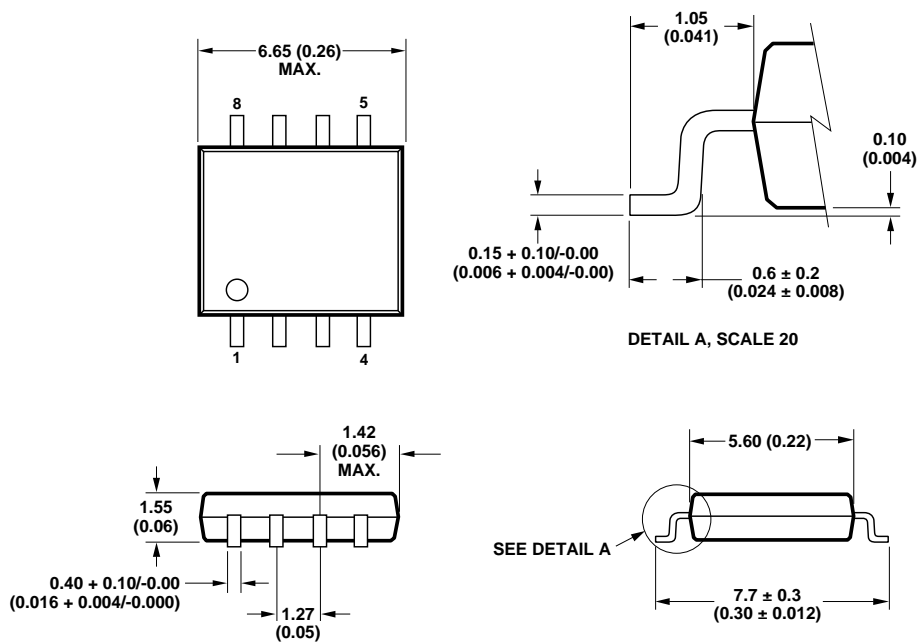
**NRST** - Active low signal used to reset the decode state machine. This signal can be tied to POR (Power on reset) or  $V_{CC}$ . This signal can also be used to disable any data reception.

**IR\_RCV** - A 3/16th pulse width input signal from the HSDL-1000. The signal is a demodulated (pulse stretched) to generate the RCV output signal.

**IR\_TXD** - This signal is the modulated 3/16ths TXD signal which is input to the HSDL-1000.

**$V_{CC}$**  - Power.

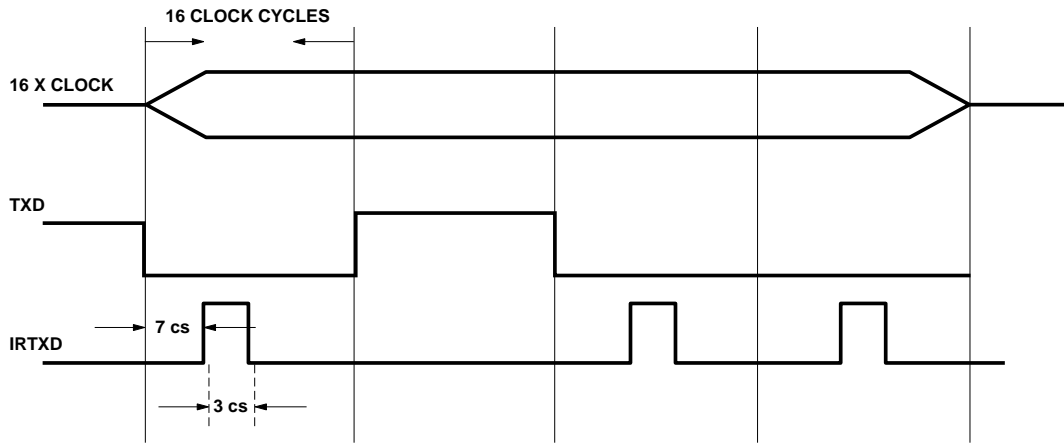
## Package Dimensions



DETAIL A, SCALE 20

NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

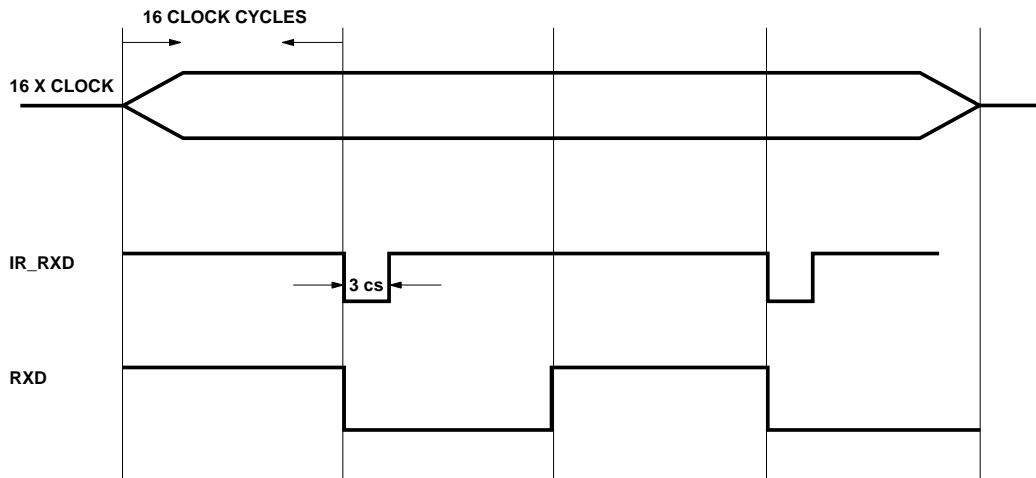
## Encoding Scheme



The encoder sends a pulse for every space or “0” that is sent on the TXD line. On a high to low transition of the TXD line, the generation of the pulse is delayed

for 7 clock cycles of the 16XCLK before the pulse is set high for 3 clock cycles (or 3/16th of a bit time) and then subsequently pulled low.

## Decoding Scheme



A high to low transition of the IR\_RXD line from the HSDL-1000 signifies a 3/16th pulse. This pulse is stretched to accommodate 1 bit time (16 clock cycles). Every pulse that is received is

translated into a “0” or space on the RXD line equal to 1 bit time.

Note: The stretched pulse must be at least 3/4 of a bit time in duration to be correctly interpreted by a UART.

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	$T_S$	-65	+150	°C	
Operating Temperature	$T_A$	-40	+85	°C	
Output Current	$I_O$		10	mA	
Power Dissipation	$P_{MAX}$		0.22	W	
Input/Output Voltage	$V_I/V_O$	-0.5	$V_{CC} + 0.5$	V	
Power Supply Voltage	$V_{CC}$	-0.5	+6.5	V	

## Switching Specifications

( $V_{CC} = 5 \text{ Volts} \pm 10\%$ ,  $T_A = -40 \text{ to } +85^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Toggle Frequency	$f_{tog}$		120		Mhz	
Propagation Delay Time	$t_{pd}$		0.5		ns	Internal Gate
			1.0		ns	Input Buffer
			2.0		ns	Output Buffer
Output Fall Time	$t_f$		1.42		ns	Output Buffer ( $C_L = 15 \text{ pF}$ )
Output Rise Time	$t_r$		1.54		ns	Output Buffer ( $C_L = 15 \text{ pF}$ )

Note:  $f_{tog}$  represents the maximum internal D-Type Flip Flop toggle rate

## Capacitance

( $V_{CC} = 0 \text{ Volts}$ ,  $T_A = -40 \text{ to } +85^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Capacitance	$C_{IN}$		10	20	pF	f = 1 MHz - Unmeasured Pins Returned to 0 Volts
Output Capacitance	$C_{OUT}$		10	20	pF	
Output Fall Time			10	20	pF	

## Recommended Operating Conditions

(T<sub>A</sub> = -40 to +85°C)

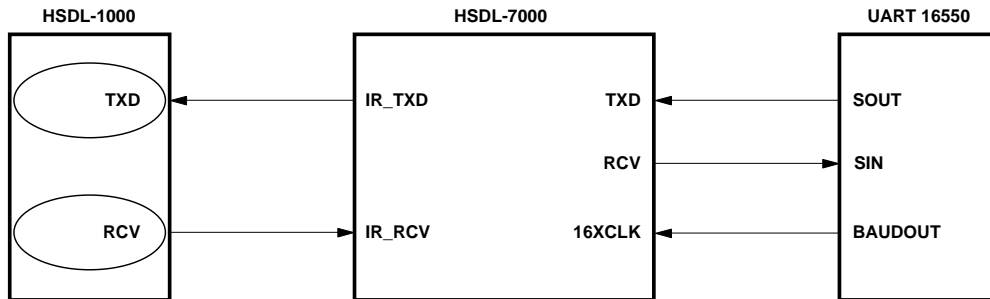
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V <sub>CC</sub>	2.7	5.0	5.5	V	CMOS level
Input Voltage	V <sub>I</sub>	0.0		V <sub>CC</sub>	V	CMOS level
Ambient Temperature	T <sub>A</sub>	-40		+85	°C	CMOS level
High Level Input Voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>		V <sub>CC</sub>	V	CMOS level
Low Level Input Voltage	V <sub>IL</sub>	0.0		0.3 V <sub>CC</sub>	V	CMOS level
Positive Trigger Voltage	V <sub>P</sub>	1.61		4.00	V	CMOS level
Negative Trigger Voltage	V <sub>N</sub>	0.55		3.10	V	CMOS level
Hysteresis Voltage	V <sub>H</sub>	0.50		2.00	V	CMOS level
Power Dissipation	P <sub>DISS</sub>		4.9	220	mW	f <sub>16XCLK</sub> = 2 MHz
Input Rise Time	t <sub>ri</sub>			200	ns	f <sub>16XCLK</sub> = 2 MHz
Input Fall Time	t <sub>fa</sub>			200	ns	f <sub>16XCLK</sub> = 2 MHz
Max Clk Frequency (16XCLK)	f <sub>16XCLK</sub>			2	MHz	
Minimum Pulse Width (IR_TXD)*	t <sub>mpx</sub>	250			ns	f <sub>16XCLK</sub> = 2 MHz

\*IrDA Parameters. The Max Clk Frequency represents the maximum clock frequency to drive the HSDL-7000's internal state machine. Under normal circumstances, this clock input should not exceed 16 \* 115.2 Kbp/s or 1.8432 MHz. This product can operate at higher clock rates, but the above is the recommended rate.

The Minimum Pulse Width represents the minimum pulse width of the encoded IR\_TXD pulse (and the IR\_RCV pulse). As per the IrDA specifications, the minimum pulse width of the IR\_TXD and IR\_RCV pulses should be 3 \* (1/1.8432 MHz) or 1.63 μs. The minimum pulse width specified for the HSDL-7000 is 250 ns, which is within IrDA specification. Under normal circumstances, the pulse width should not be less than 1.63 μs.

## Application Circuits

HSDL-7000 Connection to UART



**Note:** At the time of this publication, Light Emitting Diodes (LEDs) that are contained in this product are regulated for eye safety in Europe by the Commission for European Electrotechnical Standardization (CENELEC) EN60825-1. Please refer to Application Briefs I-008, I-009, I-015 for more information.